REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1 and 90-145 are presently pending in this application, the Specification and Claims 141-142 amended and Claims 143-145 added by way of the present amendment.

In the outstanding Office Action, the disclosure is objected to because of informalities; Claims 141 and 142 were objected to for insufficient antecedent basis; Claims 1, 90-95, 98-109, 112-115, 117-118, 120-121, 124-127, 130-131 and 133-142 were rejected under 35 U.S.C. 103(a) as being unpatentable over JP 08-172273 to Yabushita et al.; Claims 96-97, 110-111, 128-129 and 132 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yabushita et al. in view of U .S. 5,586,006 to Seyama et al.; and Claims 116, 119, 122, and 123 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yabushita et al. in view of JP 10-022601 to Hitachi.

With regard to the objection to the disclosure, the description of Figs. 13 and 15 in the specification has been amended to specify that the planar area of the pad structure is greater than the planar area of the conductive circuit. It is well settled that the drawings alone can provide adequate written description under 35 U.S.C. § 112, first paragraph. Thus, the amendments to the specification do not present an issue of new matter.

With regard to the rejection under 35 U.S.C. § 112, second paragraph, Claims 141-142 have been amended to provide antecedent basis. Thus, this rejection is also overcome by the present amendment.

I. Request for Reconsideration of Rejected Claims or Discussion of Amendments that the Examiner Deems Necessary to Clarify Distinctions Discussed Herein

Applicants respectfully submit that the rejected claims are patentable over the cited references for the reasons discussed below. While Applicants believe that the remarks

provided herein should result in allowance of the claims in their present form, the Examiner is requested to contact the undersigned Attorney of Record, Ed Garlepp, at (703) 412-5920, to discuss any amendments deemed necessary to clarify the distinctions discussed herein and place this case in condition for allowance. For example, Applicants submit that newly added Claims 142-145 provide further distinctions over the cited references and may be allowable. However, as the rejected claims in this case are ***not*** amended herein, this response cannot "necessitate a new grounds of rejection," and a ***forthcoming Office Action including the new grounds of rejection for any unamended claim cannot be properly made final.***

II. The Cited References Do Not Teach or Suggest The Features of Independent Claims 1, 103 or 124

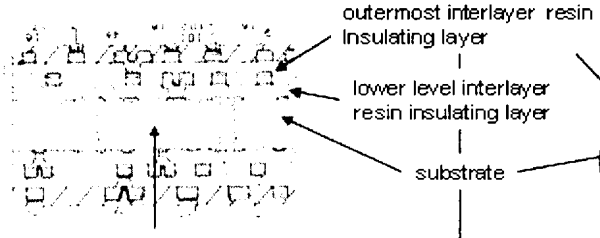
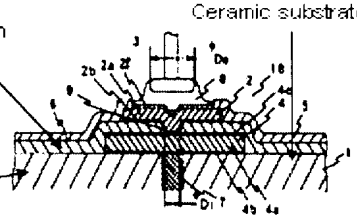
As discussed in the previous response, Claim 1 recites that the package substrate includes a lower level interlayer resin insulating layer and a lower via hole formed in the lower level interlayer resin insulating layer, and that a pad structure is formed in an outermost interlayer resin insulating layer formed over the lower level interlayer resin insulating layer. An example structure covered by this claim language is shown in Fig. 14 of Applicants original specification. As seen in this figure, the package substrate 135 includes a lower level (i.e inner level) resin insulating layer 52 having a lower via hole formed therein (in the Fig. 14, a plurality of lower level via holes are shown. As also seen, a pad structure 16 is provided in an outermost resin insulating layer (also numbered 52) formed over the lower level, and a pin 100 is provided on the pad structure 16. As discussed in Applicants' specification, this structure can prevent peeling off of the pad 16 from the resin layer 52.[1]

Before discussing Yabushita et al., Applicants first note that the outstanding rejections are based on a machine translation of Yabushita et al. Attached herewith is a human translation of Yabushita et al., which may assist the Examiner to identify the distinctions disclosed herein.

[1] US 2009/0053459 (Applicants' published specification) at paragraph 278.

Yabushita et al. discloses a mounting structure for a ceramic wiring board. As seen in Fig. 1 of this reference, the substrate 1 has a stress relaxation layer 4 formed thereon, and an insulating resin layer 6 formed directly on the substrate 1 and the stress relaxation layer 4. A solder resist 5 is then formed over the insulating layer 6, and a pad structure is formed in the solder resist layer 5 and insulating layer 6. However, Yabushita et al. does not disclose a lower level ***interlayer resin*** insulating layer having a via formed therein.

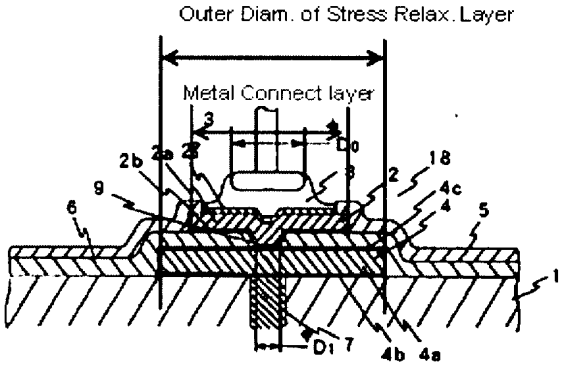
The Response to Arguments portion of the Office Action takes the position that the multilayer substrate of Yabushita et al. can form part of the interlayer resin insulating layer. However, as explained in the human translation of Yabushita et al. submitted herewith, the substrate is a ceramic substrate. Applicants respectfully submit that the ***ceramic substrate*** cannot meet the claim limitation of a lower ***interlayer resin*** insulating layer. This difference is summarized in the table below. Applicants submit that this difference alone patentably distinguishes Claim 1 over Yabushita et al. and the remaining cited references.

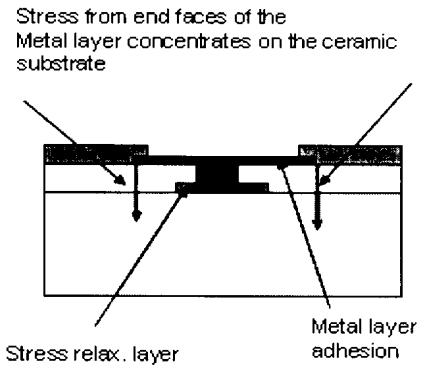
	Claimed Invention	Yabushita
resin insulating layer		 Fig.1 in Yabushita does not disclose a lower level interlayer resin insulating layer.

In addition, however, Claim 1 also recites that ***"the planar area of the pad structure is greater than the planar area of the conductive circuit."*** An example embodiment covered by this claim feature is shown in Figs. 13 and 15 of Applicants' specification. As seen therein, the planar area of the pad structure 16, defined by its opposing ends in Figs 13 and

15, is greater than the planar area of the conductor circuit 66. By contrast, Yabushita et al. clearly discloses that the pad structure 2 has a substantially smaller area than does the conductor 4.

The Response to Arguments portion of the Office Action takes the position that the relative size of the pad structure and conductive circuit cannot support patentability of the invention because the specification does not point out any significance of this feature. However, page 2, lines 5-29 of the original specification explains the prior art problem of an excessively small area of contact between the pad 716 and the interlayer resin insulating layer 752, as shown in Fig. 76. This small area permits peeling of the pad from the substrate due to, for example, warping of the substrate. Thus, Applicants' specification discloses the advantage provided by the relative area feature of the claims, and this feature is not disclosed in Yabushita et al. This provides an additional distinction over the cited reference to Yabushita et al.





The secondary references to Seyama et al. and Hitachi are cited only for teaching of the dependent claims, and these references cannot correct the deficiencies of Yabushita et al. Moreover, it would not have been obvious to one of ordinary skill in the art at the time of the present invention to modify the structure of Yabushita et al. to correct the deficiencies of this reference. As discussed in the specification, the present invention is provided in the context

of a resin substrate which is prone to warping. As such, the pad structure having the pin thereon is easily dislodged from the resin substrate. To improve this situation, the claimed the outer periphery of the pad structure is covered by the solder resist layer as noted above. Yabushita et al. does not mention the issue of a peeling pad because the base is ceramic and not prone to warping. That is, one of ordinary skill in the art would have no reason to replace the ceramic substrate with a resin substrate because this would create the problem of a peeling pad, which is what the invention is directed to addressing.

For the reasons discussed above, Claim 1 patentably defines over the cited references. Independent Claims 103 and 124 include similar features to those of Claim 1, and thus, these claims also patentably define over the cited references for the reasons stated above. Further, as dependent Claims 90-102 and 104-145 depend from either Claim 1 or 103, these claims are also allowable for substantially the same reasons set forth above for Claims 1 and 103.

III. Dependent Claims 141-145 further distinguish over the cited references

Nevertheless, dependent Claims 141 and 142 recite additional features which provide a further basis for patenting over the cited references. Each of these claims recites "wherein the pad structure connects with the conductor circuit formed on the core substrate." Further, new Claims 143-145 recite that the package substrate of Claim 1, further comprises a resin insulating substrate, wherein the lower level interlayer resin insulating layer is formed over the resin insulating substrate. The cited references also do not disclose this feature, as discussed above. Thus, these Claims provide a further basis for patentability over the cited references, and, even if Claims 1, 103 and 124 are rejected, Claims 141-145 should be indicated as allowable.

In view of the amendments and discussions presented above, the present application is believed to be in condition for allowance, and Applicants respectfully request an early and favorable action to that effect.

Respectfully submitted,

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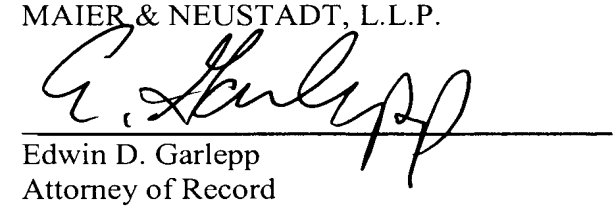
MAIER & NEUSTADT, L.L.P.



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